selecting means for establishing the delay path for the input signal by selecting one of the selecting switch sections,

wherein an output signal from the delay path has a desired delay time.

REMARKS

The above amendments and the following remarks are fully and completely responsive to the Office Action dated July 2, 2002. Claims 1-2 and 4-32 are pending in this application, with claim 3 cancelled and claim 32 added by the present amendment. In the outstanding Office Action, claim 3 was objected to; claims 1-3, 16-18, 26 and 29-31 were rejected under 35 USC §102(b); and claims 4-15, 19-25 and 27-28 were rejected under 35 USC §103(a). No new matter has been entered. Claims 1-2 and 4-32 are presented for consideration.

Claim Objections

Claim 3 was objected to. The cancellation of this claim renders this objection moot.

35 USC §102(b)

Claims 1-3, 16-18, 26 and 29-31 were rejected under 35 USC §102(b) as being anticipated by Marbot (U.S. Patent No. 5,521,540). In making this rejection, the Office Action asserts that this reference teaches each and every element of the claimed invention. Applicants request reconsideration.

Claim 1 recites a delay circuit. This circuit includes a delay section having two or more predetermined delay stages. Each predetermined delay stage adds a predetermined delay time to an input signal. The circuit also includes selecting switch sections. At least one of the selecting switch sections includes a buffer section for receiving delayed input signal from one of the delay stages and a selecting section directly connected to the buffer section for activating the buffer section to establish the delay path. The circuit also includes a selecting means for establishing the delay path for the input signal by selecting one of the selecting switch sections. Thus, the output signal from the delay path has a desired delay time.

Marbot discloses a delay circuit that includes a plurality of modules U0-U4. Each module is controlled by a respective selection signal a0-a4 and includes a charging circuit PC and a discharging circuit DC, which are controlled by the associated signal. The charging circuit PC includes a variable resistor R0* and two switches P0 and SW0*. The discharging circuit is formed by a variable resistor R0 and two switches N0 and SW0. The switches SW0 and SW0* are controlled by the selection signal a0 associated with the module U0. The variable resistors of the even-numbered modules are controlled in such a way as to assume a value that is inversely proportional to the coefficient K. The odd-numbered variable resistors are controlled in such way to assume a value inversely proportional to 1-K. When the first two modules U0 and U1 are selected, the variable resistors and the structural capacitance of the line L will define the RC time constant of the charging circuit PC and the discharging circuit DC. The coefficient K is also used to determine the voltage value to which line L will discharge to when switch N0 closes and switch P0 opens.

One object of the present invention is to accurately generate delay signals having a predetermined delay time and delay pulses having predetermined time width. These delay signals are generated by adding delay time to propagating signals derived from input signals without delay and deformation of waveform caused by parasitic elements. In particular, the present invention lets short pulses, capable of coping with high-speed operation, delay accurately without destroying the pulse waveform. In contrast, the object of Marbot is to realize "linear adjustment" with respect to delay signals.

In the present invention, a buffer section and a selecting section are directly connected to each other to reduce parasitic delays caused by resistance elements, capacitance elements or the like. Accordingly, there is no appreciable delay between the buffer section and the selecting section. In Marbot, the "variable resistor" between the "first and second switch means (P0, N0, SW0,...P4, N4, SW4)" provides "linear adjustment" in the RC time constant. The "variable resistor" has a resistance value inversely proportional to K or 1-K. K is a value between zero and one, thus, a resistance value of zero cannot be obtained. Therefore, Marbot fails to teach the direct connection recited in the present claims. Accordingly, structure of the present invention cannot be anticipated by Marbot.

In the present invention, the delay section generates delay signals. The selecting switch sections each of which includes a buffer section and a selecting section select a predetermined delay signal generated at the delay section by selectively switching the selecting section. Accordingly, only one of the selecting switch sections is selected so as to obtain desired delay signal. Consequently, this structure prevents unnecessary current from flowing between adjoining selecting switch sections, whereby low power consumption

can be realized during high-speed operation. In contrast, the desired delay signal, in Marbot, is obtained by adjusting the delay time with the CR time constant of two adjacent modules. Adjusting the delay time requires adjoining modules to concurrently conduct. However, when adjoining modules conduct concurrently, current flows from the power source to ground. Consequently, low power consumption cannot be realized with Marbot's structure.

In the present invention, the buffer section and selecting section are directly connected, and parasitic delays reduced and/or eliminated. Consequently, signals propagate in the shortest length of signal transition time. Accordingly, propagation delays of signals and deformation of signal waveforms are eliminated. Therefore, pulses having a desirable predetermined delay time can be accurately output. In contrast, Marbot, adjusts the delay time by adjusting the CR time constant in accordance with a resistance value provided for a current path formed between adjoining modules when the both of the adjoining modules concurrently conduct. In order to adjust delay time, the signal transition period between adjoining modules for each of the adjoining modules must coincide with each other. Accordingly, signal transition time at each module becomes long and short pulses cannot be propagated accurately. Therefore, Marbot teaches a variable resistor between the "buffer" and "selecting" section in order to adjust the delay time. In contrast, the present claims recite a direct connection between the "buffer" and "selecting" sections.

Consequently, Marbot fails to teach the claimed invention. Specifically, Marbot fails to teach and/or suggest a direct connection between the "buffer" and "selecting" sections; Marbot also fails to teach and/or suggest the recited selecting means. Accordingly, Applicants request reconsideration and withdrawal of the rejection under 35 USC §102(b).

35 USC §103(a)

Claims 4-15, 19-24 and 27-28 were rejected under 35 USC §103(a) as being unpatentable over Marbot. In making this rejection, the Office Action asserts that these claims are either taught or suggested by Marbot. Applicants request reconsideration.

As discussed in detail above, Marbot fails to teach and/or suggest a direct connection between the buffer section and the selection section. Marbot also fails to teach and/or suggest the recited selecting means. Therefore, Marbot fails to teach and/or suggest the claimed invention. Accordingly, Applicants request reconsideration and withdrawal of the rejection under 35 USC §103(a).

New Claim

Claim 32 is added to further claim Applicants invention. This claim is allowable for at least the reasons discussed above.

Conclusion

Applicants' amendments and remarks have clearly overcome the objection and rejections set forth in the Office Action dated July 2, 2002. Specifically, the cancellation of claim 3 renders moot. Applicants' remarks have distinguished claims 1-3, 16-18, 26 and 29-31 from Marbot and thus overcome the rejection of these claims under 35 USC §102(b). Applicants' remarks have also distinguished claims 4-15, 19-25 and 27-28 under 35 USC §103(a). New claim 32 is added to further claim Applicants invention. Accordingly, claims 1-2 and 4-32 are in condition for allowance. Therefore, Applicants respectfully request consideration and allowance of claims 1-2 and 4-32.

Applicants submit that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned Attorney by telephone, if it is believed that such contact will expedite the prosecution of the application.

The Commissioner is authorized to charge payment for any additional fees, which may be required with respect to this paper, to Deposit Account No. 01-2300 making reference to Attorney Docket No. 024016-00012.

Respectfully submitted,

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MARKED UP COPY OF AMENDED CLAIMS
S/N 09/921,561

1. (Twice Amended)A delay circuit comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a predetermined delay time to an input signal; and

selecting switch sections [for establishing a delay path for the input signal by selecting one of the selecting switch sections], wherein

at least one of the selecting switch sections comprise:

a buffer section for receiving delayed input signal from one of the delay stages; [and]

a selecting section directly connected to the buffer section for activating the buffer section to establish [the] a delay path; and

selecting means for establishing the delay path for the input signal by selecting one of the selecting switch sections, [and] wherein

an output signal from the delay path has a desired delay time.

26. (Amended) A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a predetermined delay time to an input signal; [and]

selecting switch sections [for establishing a delay path for the input signal by selecting one of the selecting switch sections], wherein at least one of the selecting switch sections comprise:

a buffer section for receiving delayed input signal from one of the delay stages; and

a selecting section directly connected to the buffer section for activating the buffer section to establish [the] a delay path;

selecting means for establishing a delay path for the input signal by selecting one of the selecting switch sections, and wherein

an output signal from the delay path has a desired delay time.

29. (Twice Amended) A delay method comprising:

a delay step in which predetermined delay times are sequentially added onto an input signal to obtain delay signals;

a selecting step which is activated to obtain [when] one of the delay signals in the delay step which has a desired delay time; and

an output step in which one of the delay signals in the delay step is output by activating the selecting step.